Amendment to the Drawings:

The attached sheet of drawings includes changes to Fig. 3. This sheet, which includes Fig. 3-5, replaces the original sheet including Fig. 3-5. In Figure 3, previously omitted element 23 has been added.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

Claims 1-22 remain in this application. Claims 1 and 11 have been amended.

In view of the above amendments and the following remarks, favorable reconsideration of the outstanding office action is respectfully requested.

§ 103 Rejections

The Examiner has rejected claims 1, 3, 5, 6, 8-10 under 35 U.S.C. § 103 as being unpatentable for obviousness over U.S. Patent No. 6,353,690 (Kulishov) in light of U.S. Patent No. 4,750,800 (Fournier et al.).

Applicant respectfully submits that the Examiner has missed some important differences between Applicant's invention, particularly as described in currently amended claim 1, and both the Kulishov and Fournier references. For starters, the Examiner asserts that Kulishov discloses an integrated optical chip having a crystalline structure cut along parallel principal crystallographic planes. Actually, there is no description whatsoever within Kulishov of the crystalline structure of the optical chip or of its orientation with respect to the principal crystallographic planes of the material from which it has been cut. Applicant has amended claim 1 to emphasize the fact that both the optical chip itself and the substrate to which it is attached have the same crystallographic orientation.

Next, given the problems that the present invention is addressing, there is nothing in either the Kulishov or the Fournier reference that would suggest that combining the structures shown in the two references would address that same problem.

The present invention addresses two countervailing considerations: first, to reduce the thickness of the integrated optical chip, in order to reduce transverse resonance within the chip substrate, which is attributed to coupling between the fundamental coplanar waveguide mode and a substrate mode and which in turn varies with the thickness of the

chip substrate (see application paragraph 0004); second, to prevent the chip from becoming so thin and fragile that it is unable to withstand the rigors of manufacturing processes (see application paragraph 0005). The present invention solves this problem by using a composite chip, in which the active chip layer 33 is reduced to a thickness that minimizes or eliminates the transverse resonance problem and is mounted onto a substrate layer 35 that provides the requisite physical strength yet, because of the isolation provided by the intervening conductive coating 13, does not contribute to the transverse resonance problem (see application paragraph 0031).

At the same time, in the present invention there is no need for the substrate layer 35 to be any thicker than is necessary to provide the requisite physical strength of the composite structure. For example, as described in paragraph 0031 of the application, a composite chip having a total thickness of around 1.0mm (i.e., the combined thicknesses of the chip layer, the substrate layer and the intervening conductive coating) is capable of operating effectively at frequencies in excess of 10GHZ, yet it also has sufficient strength to withstand rigorous shock testing..

Turning now to the Kulishov and Fournier references, there is no discussion in either of them about mode coupling, transverse resonance or physical fragility of the chips. There is no mention in either Kulishov or Fournier about the need to minimize chip thickness to avoid a transverse resonance problem. There is no mention in Kulishov of the intervening electrically conductive layer acting as a barrier to isolate the electro-optic material 24 from adverse effects introduced by the underlying substrate. Kulishov does not put any constraints on the thickness of the underlying substrate, on the relative thicknesses of the electro-optic slab and the substrate or on the total thickness of the composite structure formed by the combination of the slab and the substrate. Furthermore, Fournier states that it is desirable to have a substrate thickness that is a minimum of 10 times as thick as the optical chip to which it is attached (column 4, lines 10-14). This is totally inconsistent with the teachings of the present invention, where minimizing the overall thickness of the composite chip is an important consideration. So,

why would a person of ordinary skill be inclined or motivated to combine the teachings of these two disparate references in order to solve the problems addressed by the present invention and thus arrive at the unique present invention?

The present invention also seeks to avoid errors and distortion produced by charge differentials across the face of the chip caused by the pyroelectric effect (see application paragraph 0007). The electrically conductive coating 13 achieves this by preventing the development of such charge differentials, i.e., by allowing any charges that may occur on the surfaces of either the chip layer 33 or the substrate layer 35 to freely migrate through the conductive layer, and not to accumulate or become localized on those surfaces. This would prevent any disadvantageous electric field from being created across the chip surface.

On the other hand, the metallized layer of Kulishov performs the exact opposite function, as described at column 8, lines 36-39 of that reference. The metallized layer functions as an electrode for intentionally imposing an electric field on the optical waveguide formed within the electro-optic material.

Furthermore, since the metallized layer of Fig. 9c of Kulishov is separated from the electro-optic slab by a buffer layer made of a dielectric material (column 7, lines 1-5), the metallized layer would be incapable of dissipating any detrimental electrical charges forming on the surface of the electro-optic slab. In fact, since the buffer layer is a dielectric material, it could exacerbate the charge differential problem that the present invention is intended to prevent.

Since claim 1 (as amended) is now clearly distinguishable over the teachings of the Kulishov and Fournier references and is not obvious in view of a combination of those references, then, claims 3, 5, 6 and 8-10, all of which are dependent directly or indirectly on claim 1, by definition cannot be deemed obvious. So, there is no need for Applicant to specifically address the Examiner's obviousness rejections of those dependent claims. For the same reason, there is no need for Applicant to specifically address the obviousness rejections of dependent claim 2 (in paragraphs 10-13 of the Office Action) or dependent claims 4 and 7 (in paragraphs 14-17).

The Examiner has rejected claims 11-22 under 35 U.S.C. § 103 as being unpatentable for obviousness over Kulishov in light of Fournier et al., Shaw et al. and Shafer et al.

With respect to claim 11, many of the same reasons given above for refuting the obviousness of claim 1 (as amended) over the combination of the Kulishov and Fournier references also support Applicant's contention that claim 11 (as amended) similarly is not obvious over the Kulishov, Fournier, Shaw and Shafer references.

First of all, Applicant would like to point out that claim 11 (both in its original and amended forms) does not mention the use of adhesive to attach the chip to the substrate. Therefore, the Examiner's comments in paragraphs 20-22 related to such use of an adhesive has no relevance to the allowability of claim 11.

Echoing the comments made above with respect to claim 1, Applicant submits that, despite the Examiner's assertion, Kulishov does not contain any description whatsoever of the crystalline structure of the optical chip or of its orientation with respect to the principal crystallographic planes of the material from which it has been cut. As was the case of claim 1, Applicant has amended claim 11 to emphasize the fact that both the crystalline wafer itself and the substrate to which it is attached have the same crystallographic orientation.

Similarly, the reasons offered above with respect to claim 1, regarding (a) minimizing the overall thickness of the composite chip and (b) the functioning of the electrically conductive layer both to provide isolation from the underlying substrate (so as to avoid the transverse resonance problem) and to counteract the pyroelectric effect, also apply to claim 11 as amended.

Therefore, given that the structure of the composite optical chip being fabricated by the method of claim 11 (as amended) is now clearly distinguishable over the combination of the Kulishov and Fournier references, then the method itself of making that specific chip must be nonobvious even over the further combination with the Shaw and Shafer references. Furthermore, given that claim 11 has now been established as being nonobvious, each of claims 12-22, which are directly or indirectly dependent on

claim 11, are inherently nonobvious as well, notwithstanding the combination of references cited by the Examiner.

Based upon the above amendments, remarks, and papers of records, Applicant believes the pending claims of the above-captioned application are in allowable form and patentable over the prior art of record. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Applicant believes that a one-month extension of time is necessary to make this Reply timely. Therefore, Applicant hereby respectfully requests that the Office grant such time extension pursuant to 37 C.F.R. § 1.136(a) as necessary to make this Reply timely, and authorizes the Office to charge the fee with respect to said time extension to Deposit Account 03-3325. Should applicant be in error, and should any additional fees or surcharges be due, Applicant hereby authorizes the Office to charge such additional fees to the Deposit Account.

Please direct any questions or comments to Ronald J. Paglierani at (607) 974-3332.

Respectfully submitted,

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